CLAIMS

1. A semiconductor device having a plurality of pads above a main surface of a semiconductor substrate as terminals for external connection, wherein

the plurality of pads include dual use pads which are used in both a probing test and assembly, and assembly pads which are not used in the probing test,

the dual use pads are provided in a first area above the main surface of the semiconductor substrate, an application of pressure by a probe during the probing test being permitted in the first area, and

the assembly pads are provided in a second area above the main surface of the semiconductor substrate, the application of pressure by the probe during the probing test being not permitted in the second area.

2. The semiconductor device of Claim 1, wherein the dual use pads have a shape compatible with both assembly and connection with the probe, and the assembly pads have a shape compatible with only assembly.

3. The semiconductor device of Claim 1, wherein the first area corresponds to an area above a peripheral region of the main surface of the semiconductor substrate, and the dual use pads are arranged linearly along a periphery of the main surface of the semiconductor substrate.

4. The semiconductor device of Claim 1, wherein the

plurality of pads further include probing test pads which are not used in assembly, and the probing test pads are further provided in the first area.

5. The semiconductor device of Claim 4, wherein

the dual use pads have a shape compatible with both assembly and connection with the probe,

the assembly pads have a shape compatible with only assembly,

the probing test pads have a shape compatible with only connection with the probe, and

a measurement in a pad pitch direction of the shape compatible with only connection with the probe is smaller than a measurement in a pad pitch direction of the shape compatible with only assembly.

6. The semiconductor device of Claim 3, wherein the first area corresponds to the area above the peripheral region of the main surface of the semiconductor substrate, and the dual use pads and the probing test pads are arranged alternately and along the periphery of the main surface of the semiconductor substrate.

7. A semiconductor device having a plurality of connection pads that are terminals for external connection positioned in a top layer above a main surface of a semiconductor substrate, and at least one wiring pad positioned in an inner layer between the semiconductor substrate and the connection

pads, wherein

in an overlap area, being a portion where the at least one wiring pad overlaps part or all of the connection pads when viewed from the main surface of the semiconductor substrate, a potential of the wiring pad is the same as a potential of the connection pads.

8. The semiconductor device of Claim 7, wherein the connection pads are dual use pads used in both a probing test and assembly, whose shape is compatible with both assembly and connection with a probe.

9. The semiconductor device of Claim 7, wherein the at least one wiring pad in the overlap area is connected to a drain of a transistor formed in the semiconductor substrate, and a shape of the overlap area is substantially the same as the shape of the connection pads.

10. The semiconductor device of Claim 7, wherein a connection of a transistor gate is extended by a thin film formed on a surface of the semiconductor substrate at the portion which overlaps a connection pad, and by the at least one wiring pad at a portion which does not overlap the connection pads.

11. The semiconductor device of Claim 7, wherein the connection pads are composed of a portion used in the probing test and another portion, and the overlap area is a portion

where the at least one wiring pad and the portion used in the probing test overlap when viewed from the main surface of the semiconductor substrate.

12. The semiconductor device of Claim 11, wherein the connection pads are dual use pads used in both the probing test and assembly, a shape of the portion used in the probing test is compatible with connection with the probe, and a shape of a portion used in assembly is compatible with only assembly.

13. The semiconductor device of Claim 7, wherein the at least one wiring pad has two layers, and a via is not formed between a first and second layer of the portion where the at least one wiring pad and the connection pads overlap when viewed from the main surface of the semiconductor substrate.